Patent Claims

1. A method for reading or storing a state from or in a ferroelectric transistor in a memory cell which is arranged in a memory matrix having a number of further memory cells with further ferroelectric transistors,
   - in which the state is read from the ferroelectric transistor or is stored in the ferroelectric transistor, and
   - in which, if there is at least one further ferroelectric transistor in the memory matrix, the threshold voltage of the further ferroelectric transistor is increased.

2. The method as claimed in claim 1,
in which the state is read from the ferroelectric transistor or is stored in the ferroelectric transistor by a read/store voltage being applied to the gate electrode of the ferroelectric transistor in order to read or store the state.

3. The method as claimed in claim 1 or 2,
in which the threshold voltage of the further ferroelectric transistor is increased by applying a drain-substrate voltage to the further ferroelectric transistor in the memory matrix.

4. The method as claimed in one of claims 1 to 3,
in which a number of transistors are used in at least one memory cell in the memory matrix.

5. The method as claimed in claim 3 or 4,
in which a voltage of approximately ± 3.3 volts is used as the drain-substrate voltage.

6. A memory matrix having

- a number of memory cells which are connected to one another, with at least some of the memory cells having at least one ferroelectric transistor,
- a read/store control apparatus, which controls the process of reading or storing a state from or in a ferroelectric transistor in a memory cell in the memory matrix,
- with the read/store control apparatus being set up such that the state is read from the ferroelectric transistor or is stored in the ferroelectric transistor, and
- wherein, if there is at least one further ferroelectric transistor in the memory matrix, the threshold voltage of the further ferroelectric transistor is increased.

7. The memory matrix as claimed in claim 6, in which the read/store control apparatus is set up such that a read/store voltage is applied to the gate electrode of the ferroelectric transistor in order to read or store the state.

8. The memory matrix as claimed in claim 6 or 7, in which the read/store control apparatus is set up such that a drain-substrate voltage is applied to the further ferroelectric transistor in the memory matrix in order to increase the threshold voltage of the further ferroelectric transistor.

9. The memory matrix as claimed in one of claims 6 to 8, in which at least one memory cell in the memory matrix has a number of transistors.

10. The memory matrix as claimed in claim 8 or 9, in which the read/store control apparatus is set up such that a voltage of approximately

± 3.3 volts is used as the drain-substrate voltage.